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Amkor: 40+ years of Packaging Innovation

Amkor was founded in West Chester, PA in 1968 by the Korean Anam group who’s business model was to allow OEMs to receive efficiencies of scale by outsourcing their IC assembly and test. Amkor’s rapid growth in their semiconductor packaging services in the early 1990s was due to the rapid growth in home computers, cell phones, and other consumer electronics. Sales of $442 million in 1993 grew to $1.2 billion by 1996 (1/3 of the total semiconductor packaging market). Amkor reported sales of $2.8B in 2011. Behind only ASE, Amkor is today the number two player in packaging revenue in the world.

Amkor went public in 1998. Amkor began operations in Japan in 2001 after acquiring a packaging and test facility from Toshiba. The same year, Amkor gained access to Taiwan by investing in Taiwan Semiconductor Technology Corporation and Sampo Semiconductor. In 2002, Amkor acquired the Japanese semiconductor packaging business of Citizen Watch. The acquisition of key technical personnel, over the last two decades, has allowed Amkor to progress from a company, acquiring key technologies and scaling them into HVM, to one of today’s leading packaging innovators.

Amkor was the first of the OSATS to recognize the profound influence the Motorola OMPAC was going the have on the industry and began commercializing the BGA and supplying it to Motorola in 1993.

In 2000, Amkor licensed FCT (Flip Chip Technologies) Flex-on-Cap wafer bumping and redistribution technologies and MCNC’s (Microelectronics Center of NC) plated bumping technology, becoming the first OSAT to enter the HVM bumping market segment. In 2001, Amkor licensed FCT’s UltraCSP™ technology and the WLP (Wafer Level Packaging) era began. In 2004, Amkor acquired Unitive, a bumping spin-off of MCNC, and their production site in Taiwan. With this acquisition, Amkor gained qualified, high volume wafer bumping and chip scale packaging manufacturing operations in Taiwan.

In 2005, Amkor introduced the stackable, very-thin, fine-pitch BGA, the base of their high density platform for PoP (Package-on-Package) stacking. In 2009, Amkor introduced its next generation PoP technology, TMV® (Through Mold Via) which creates interconnect vias through the mold cap.

In 2010, Amkor and Texas Instruments announced the qualification and production of the industry’s first fine pitch copper pillar flip chip packages. Also in 2010, Xilinx announced their most advanced Virtex-7 FPGA, the industry’s first silicon interposer product with TSV. Die bumping and module assembly was done by Amkor.

Amkor is today a leader in IC packaging development and manufacturing with more than 850 different IC packages. Therefore, this special edition of Yole Développement’s “3D Packaging” will share with our readers several of the technologies that Amkor have put, or are in the process of putting, into place.

Dr Phil Garrou, Senior Analyst, Yole Développement

...The acquisition of key technical personnel, over the last two decades, has allowed Amkor to progress from a company, acquiring key technologies and scaling them into HVM, to one of today’s leading packaging innovators....
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System integration ups the ante: Amkor leadership positions for a changing packaging industry

The proliferating options for system integration are driving change across the packaging industry, requiring more investment in developing, ramping and supporting new die-, wafer- and board-level solutions. Amkor counts on its solid base of platform technologies to ease transition to this next generation.

System integration is the key issue driving the packaging sector, with integration at the board, wafer, and die level happening simultaneously, notes Ron Huemoeller, Amkor SVP of Advanced Product Development. Although disruptive changes are afoot in all these areas, the basic platforms and accumulated learnings for handling common issues like thinning, warpage and chip/package interactions are largely already in place. "All the resources and money we’ve put into packaging technology for the smart phone has quietly built up a strong infrastructure for the future,” adds ChoonHeung Lee, Corporate VP of Product Management.

Groundwork laid for proliferating integration options

How can an OSAT drive more functionality per package today? At the board level, embedded passives are now mainstream while embedded active die are less common as PCB technology is still being improved. While embedded die packaging allows higher density and more I/Os than the through-mold-via approach, the less tightly controlled PCB technology means higher yield loss. The key to extending the PCB based packaging to more applications will be improving the yields while limiting the cost adder. The primary approach for reducing this loss is to add the die at the very end of the process in a cavity on the top side of the substrate. Unfortunately, however, making cavities in laminate substrate remains expensive. To address the needs of next generation board integration, substrate suppliers will also have to step up their investment in development to extend the technology from 15µm down to possibly <5µm lines and spaces. This will require improvements in lithography and in materials, perhaps going to thinner roll-to-roll processable materials or glass. As a result, integration on silicon or glass interposers now looks like the more viable option for many applications,
particularly for larger, more expensive die. Ultimately, cost will be the final determination of which technology choice is used for advanced package integration approaches.

"System integration is the key issue driving the packaging sector, with integration at the board, wafer, and die level happening simultaneously," notes Ron Huemoeller.

"At the wafer level, fan-out wafer-level packaging remains a niche market," notes Robert Lanzone, SVP of Advanced Engineering Services. The single and dual die Wafer-Level Fan-Out (WLFO) devices, however, have helped develop processes for die placement, singulation, wafer and mold thinning, warpage mitigation, and handling chip/package interactions, all common elements necessary for future platforms for stacking die. The 3D extension of the WLFO platform may help expand its market potential, and recent developments in laser direct write may help to significantly reduce costs.

At the die level, coming next will likely be transitional technologies for die-to-die stacking on a single platform. One solution now in development at Amkor for possible production near term is a hybrid die stacking technology that extends flip chip towards the TSV space to increase bandwidth and decrease signal latency. Descriptively called POSSUM™, the approach flip chips a mother chip with a thin daughter chip hanging underneath, then flip chips the mother chip to the substrate. For example, this approach can connect a controller directly to an ASIC without having to go through a substrate.

"Amkor has most of the platform technologies in place for the future TSV and interposer packaging technologies, several of them developed for the fine pitch copper pillar and other technologies," says Lanzone, noting thermal compression attach, ultra thin silicon, dicing of thin silicon, and bonding/debonding platforms. "Now we need to focus on how to bring down the cost. Though 3D is coming in at the high end, it will only advance when costs are at par or lower to accelerate adoption."

Through-silicon vias will at last become the big play for advanced system integration in two to four years, with silicon interposers, or perhaps glass at some I/O nodes, used widely, suggests Huemoeller. "Our customers prefer the interposer path because it has the potential to decrease die size, motherboard size and layer count," he notes. "Though the package cost may increase, it provides a path to savings at the systems level." The industry seems to be settling around making the fab to assembly and packaging handoff with full thickness wafers, to manage the bond and debond steps at the same facility, as the OSATs gain sufficient experience in wafer bonding and thinning.

Any move to 450mm wafers may slow adoption of fully 3D TSV into logic die, but it won’t slow adoption of the interposer platform. Though silicon interposers, with their well established silicon infrastructure, will be used first, Huemoeller notes improvements to via cost and die singulation on glass interposers are progressing, though issues with process maturity remain. "If progress continues at the same rate we’ve seen over the last year, glass interposers could become reality," he adds. "That is, if a sufficient supply base becomes convinced of returns from investing in support of large format glass."

Testing, however, remains a major issue. Lee notes the problems of defect analysis on a 3D device with 50,000 microbonds on 45µm pitch
on 50um via pads for each of four dies. "We can't grind down the device to look at 200,000 bonds, we have to use FIB microscopy instead," he says, noting that how to probe these devices is still only at the R&D stage, and the industry will need statistical approaches and low cost solutions for high volume manufacture.

Amkor figures large OSATs have the long-term edge in the middle-end

Besides the learnings from all the pre full 3D TSV system integration approaches, major OSATs may also be both more experienced and more willing to keep investing in the emerging "middle-end" process flows, which are likely to have margins closer to the back-end assembly business than to those of the front end fabs.

"Not only is it heavily capital intensive just to step in to these new middle-end technologies, but it will take continued investment over the next 5-10 years to stay relevant," says Huemoeller. "We invest hundreds of millions of dollars every year as a company to remain competitive and find differentiated advantage in the assembly space. The foundries have to be willing to do this as well, knowing it will weigh heavily on their bottom lines. Will their boards allow them to keep investing in this relatively lower margin business long term?" He notes that the foundries have had to spend more upfront than the OSATs, since the OSATs have been able to re-use more of the assembly assets they already own. All players also have to build the expertise to work with the customer early on in package design and die layout. Though high-end devices and best yields will likely drive the 3D IC business initially, in the long term industry yields usually all level out, and then the sector will be driven by cost. IDMs will stay in the business as long as they see differentiation, but as the new technology matures, they will more likely shift to outsourcing to reduce costs. "Will the foundries be willing to keep lowering their package pricing to remain competitive?" asks Huemoeller.

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Now that the OSATs and foundries have learned that transferring thin wafers can only result in disagreements on what is a good incoming product, and that bonding and debonding need to be done at the same site, the options for handoff have narrowed to shipping full thickness wafers. That's pushed TSMC to apparently now plan to keep the entire TSV packaging and assembly process in house. "But the issue is no customer wants to give up control over both, their pricing and their roadmap by relying entirely on one company," says Lee. TSMC may plan to concentrate on the high end applications, offering interposers as an interim solution for its customers to help them extend the performance of the 28nm node in the face of potential delays and high costs of 20nm lithography.

UCM and GLOBALFOUNDRIES, on the other hand, prefer to stay out of the back end business, so reportedly plan to ship the unthinned TSV wafers to the OSAT and leave the complete middle-end process to them. "UMC sees no benefit in doing assembly where it has no expertise and margins are lower," notes Lee. That leaves the OSATs with the challenge of investing significantly and learning to master the complex CMP fab process for TSV via reveal, where the foundries already have both the facilities and the experience, but the packaging side has the most expertise in the rest of the flow.

Key is careful investment in core platform technologies for multiple volume markets

Amkor counts on careful selection of platforms that will have wide application. "We really study the value proposition before we spend a lot on developing the technology," says Lanzone. "Our value-added is making technologies broadly applicable, to multiple different segments, so we can scale them to volume. We work with our customers to drive their requirements to scalable solutions." He notes the company's caution in investing in standard single chip wafer-level fan out, for example, where several years ago, the company spent six months designing and costing out the technology against possible alternative packages, and found few applications where it would be competitive. Amkor also counts on customers seeing ways to make use of technology platforms for new applications, for example, with the POSSUM™ chip-on-chip technology. Originally used to attach a MEMS die to an ASIC, it turns out to also have use as a low cost wafer-level package approach for high speed applications like gaming.

Copper pillars and thermal compression bonding turn out to have particularly wide application for both better performance and lower cost. They will increasingly replace flip chip where the older technology is challenged to get to narrower pitches for 20nm devices, or to maintain reliability on bigger die or those with brittle low-k layers, says Lee. At the other end of the spectrum, more companies are choosing them as a lower cost replacement for wire bonding for higher density on smaller die.

And steadily shaving off microns and pennies

A big part of making a platform meet the needs of a range of applications to drive it to high volumes is of course to drive down its costs. For fine pitch copper pillar bumping, Amkor and development partner Texas Instruments targeted low cost from the beginning to compete with wire bonding. That meant figuring out how to eliminate the passivation/repassivation layer and make the bumps directly on the Al pad, to reduce the process to a single
mask step, although some customers were reluctant to skip that familiar process initially. Amkor ran two alternative lines for a year, one with mass reflow and one using thermal compression bonding, as it figured out how to deal with the warpage of the state-of-the-art <100µm die that challenged attachment yields. But the result was a major reduction in bump pitch in 18 months. "We literally leapfrogged 150µm solder bumping to move to 50µm," says Lanzone. Now the roadmap is the more typical incremental driving down pitch from 40/80µm to 30/60µm next and 20µm pitch in the future. "Most of what we do is shave off tens of microns," notes Lanzone.

A similar effort is also underway to reduce the cost and extend the addressable market for wafer-level and chip-size packaging platforms to larger die, while still meeting reliability requirements when put on the PCB directly without underfill. There Amkor engineers have reduced the original four-mask process down to two, by eliminating a polymer passivation step and the under-ball metatilization layer, and are working on developing a new deposition technology to decrease the capital cost structure as well.

The company also counts on its through-mold via platform to reduce the height of PoP stacks, while also increasing the interconnect pitch density and managing the thin die warp for mobile applications. The dies are overmolded capped, then laser ablated, to gradually reduce the thickness of the cap. Film-assist molding—putting thin Teflon-like film between the die and the mold compound—means the top of the die can be selectively kept bare of compound, to keep the package as thin as possible, as well as to allow the possibility of easier thermal management.

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**Ron Huemoeller, Senior Vice President, Advanced Product Development, Amkor Technology**

Ron joined Amkor in 1995, and has served in various senior management roles. He is currently responsible for corporate strategy, business development and commercialization of advanced products and technology platforms. Prior to joining Amkor, Ron was Director of Engineering at Cray Computer. He holds a degree in chemistry from Augsburg College, a Masters in technology management from University of Phoenix and an MBA from Arizona State University.

**Robert Lanzone, Senior Vice President, Advanced Engineering Services, Amkor Technology**

Bob joined Amkor in 2004, he is responsible for Amkor’s engineering services that include thermal, mechanical, and electrical design, finite element modeling and testing along with wafer level package development. Bob has served in various corporate business development and vice-president positions and was responsible for Amkor’s Fine Pitch Flip Chip, Copper Pillar and next generation Package on Package TMV® developments. He previously worked for IBM, Kyocera, Unitive and ChipPAC. Bob holds a mechanical engineering degree from Polytechnic University (NYU).

**ChoonHeung Lee, Corporate Vice President, Product Management, Amkor Technology**

ChoonHeung joined Amkor in 1996 as the Team Manager of the Simulation and Advanced Product Development group, and in 2010 was promoted to Head of Corporate Technology. Choon has written 23 research papers on various packaging technology related subjects and has been granted 26 patents in Korea and 11 in the US. Choon holds a degree in physics and a Masters degree in statistical physics from Korea University and a Masters degree and Ph.D. in physics from Case Western Reserve University.
Consumer markets drive MEMS packaging towards outsourcing, standard platforms

The high volumes, fast cycle times and severe cost pressures of consumer electronics markets are driving MEMS device makers away from their traditional custom approach of one product, one process, one package, and towards the kinds of fast product ramps and lowest cost production traditionally enabled by the OSATs.

“Amkor is addressing this market’s needs with mature volume packaging lines and testing services, and flexible standard package platforms that can handle everything from inertial sensors, pressure sensors, and microphones to the newest emerging sensor applications.

“What we observe is that high volumes, short cycle times, and lower costs are driving the IDMs toward more standard platforms,” says Adrian Arcedera, Amkor Senior Director, MEMS & Sensor Products. Although the fabless MEMS makers have always been first to adopt the standard packages offered by OSATs, even the big IDMs who largely dominate the MEMS business with more custom designs are being driven by volume consumer markets to outsource more packaging, assembly and test. Outsourcing allows the IDMs to focus more of their capex on the front end, and leverage backend flexibility and risk mitigation with second sources for packaging. “Our customers want the ability to expand to meet MEMS growth, so more business is coming our way,” Arcedera notes. “The IDMs have more defined requirements because they have years of expertise and perhaps more custom expectations, but if they want high volume and fast cycle times and lower costs, it drives them to a standard package also.”

Fast growth and high packaging costs make the MEMS market ripe for change, and a ripe opportunity for those who can enable it. Unit demand is growing at 20% CAGR, more than twice the growth rate of IC package units, according to Yole Développement. Consumer applications—and specifically the accelerometers, gyroscopes, magnetometers and microphones used in mobile devices—increasingly dominate the business, and now account for more than 50% of MEMS units shipped. Yole figures packaging, assembly and test offer the most headroom for cost reduction, as they account for a major portion of total manufacturing costs, some 35%-45% for a typical accelerometer, for example. And with MEMS devices moving quickly to tighter integration of multiple sensors and smarter processing, the contribution of assembly, packaging and test costs will likely become even more significant.

Standard package platforms allow quick product ramps

Amkor offers two standard package platforms, one based on a MicroLeadFrame® (MLF), the other on a laminate or ceramic substrate, each topped with a metal or a plastic lid that creates a cavity around...
the MEMS device for a low stress environment where the molding compound is not in contact with the sensors. Ports can be opened in either the top or bottom, die can be side by side or stacked, wirebonded or bumped. The devices can also be fully overmolded if less sensitive to stresses – or molded in-cavity to expose die surfaces to the environment. All are assembled on dedicated lines converted from mature, high capacity production lines. The production lines have been modified to handle the wide variations in materials for MEMS devices and they lend themselves to cleaner handling and better particle control for the uncapped MEMS devices.

“We tend to be pulled in earlier for MEMS designs,” says Russell Shumway, Director, MEMS & Sensor Products, noting the need to adjust the packaging approach and materials for specific products’ different sensitivities to stress. “Amkor has put effort into building the capability to simulate RF, electrical and thermo-mechanical stresses, which is then used to specify the appropriate low stress materials,” he adds. “We have also worked on building a strong supply chain for what used to be relatively exotic materials.”

Standardization, where appropriate, speeds package design, and especially re-design for the next generation device. “The cavity isolates the MEMS die from the stress compared to using a molding compound, so a designer can sometimes re-use the same package with different MEMS devices, even as different as a microphone and a pressure sensor,” notes Shumway. “And the next generation device can keep the same package footprint dictated by the OEM.”

“We’re working now on packaging combo sensors,” adds Arcedera. “The cavity packages are good for multiple sensors that may have different stress levels.” The platforms also allow selective application of molding compound at the end of the process line, by a roll-to-roll film-assist process that puts fresh film between the device and the mold cavity to prevent the compound sticking to the surface of the die, or to create a cavity for placement of another die, useful for things like tire pressure monitoring systems, humidity sensors and fingerprint sensors.

**Next generation solutions move to flip chip, bumping**

New MEMS devices, in new kinds of packages, are also poised for growth. Silicon MEMS oscillators, with their convenient custom tunability, are seeing wider acceptance for replacing traditional quartz timing devices, and more players are entering the market. Amkor is seeing demand for MEMS timing devices packaged in chip-on-chip technology, which joins MEMS and ASIC die face to face, initially with solder balls, but potentially with copper pillar bumps for higher densities, reports Jemmy Sutanto, Senior Manager, Advanced Package Development. This approach reduces package size and improves signal speeds, bandwidth and latency between the two devices, at assembly costs that may be comparable to wire bonding at high volumes. Though the first MEMS timing devices got customer acceptance by putting the small MEMS units into the same traditional low cost plastic MLF (aka QFN) packages used for existing quartz devices for drop-in replacement, Sutanto says some entrants are now jumping directly into wafer level packages for large volumes.

In one approach to face-to-face chip-on-chip packaging, which Amkor calls the POSSUM™ configuration, the larger of the attached pair of chips is then flip-chipped onto a substrate or even directly to a motherboard as either a WL CSP or a BGA. Eliminating the need for a substrate to carry signals between die will significantly reduce the MEMS packaging cost. “We fully expect chip-on-chip approaches to be adopted for accelerometers, gyroscopes and RF multi-chip assemblies” states Sutanto (as illustrated in Figure 2). “We’re starting with simpler, low density devices, but this is potentially a very significant market.”

Though wire bonding still continues to dominate the MEMS packaging market, Amkor notes it’s now seeing more discussion of flip-chip to decrease the size of the device, and improve parasitic resistance and latency.

“It’s a classic chicken and egg problem,” notes Sutanto. “MEMS needs better solutions to drive down the high cost of packaging, but it takes billions of units to really drive down costs. So how to get there takes some courage. The costs of the best long term solution might be a little higher at first. We’re really looking for the long term solution.” The POSSUM™ configuration is a potential enabling technology toward low cost 3D packaging integration, states Sutanto. Adrian Arcedera continues, “the trend of electronics is toward functional integration, whether in the silicon as a SoC or in the package as a SiP. Package integration extends choice to our customers.”

**More MEMS testing moves to OSATs too**

Amkor says consumer devices’ demand for high volume manufacturing efficiencies is also driving more once-proprietary MEMS testing to the OSATs, as well as driving more attention to smart design for test. IDMs are increasingly outsourcing their consumer device testing, since their plants are overflowing, though they may keep their more delicate, higher-touch testing in house. Good design for test helps differentiate MEMS devices, by reducing test time and cost, notes Mark Berry, Vice President, Test Sales Manager. “Customers used to come with their own test, but with the low cost drivers of the consumer market we see a lot more interest in early collaboration for test design,” he says.

That’s also driven Amkor into the test equipment business. Though flip-and-spin motion handlers for testing inertial sensors are commercially available, many other
types of practical high volume commercial sensor testing equipment are not. So Amkor has devised stimulus and sensing modules to bolt on to existing high speed handlers, suitable for high volume testing of magnetometers or RF or microphones, with relatively low additional capital equipment cost. The same handlers can then later be used with other modules as needs change or as higher parallelism is required.

Complex testing of advanced devices could also drive more testing to the OSATs. Distributed testing at the wafer-level or earlier in the process flow can improve results with more advanced devices, and that means more testing done during packaging. Innovative approaches such as doing wafer level probe to create motion and characterize the settling time, then correlating that to the rejection and control limits, or other options to replace mechanical testing with electrical test in mature, well characterized devices, may also change the traditional testing process.”MEMS testing swings the pendulum of value towards the backend,” notes Berry.
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The importance of test in packaging: a MEMS/electronic sensor case study

The test process can improve yield through the recovery of low sensitivity parts or through powerful algorithms that compensate for assembly equipment errors, thus providing value-add and direct impact to the bottom line,” explains Gerard John, Amkor Technology.

Today’s smart devices focus on the Degrees of Freedom (DoF) offered to the user. With the introduction of Micro Electro-Mechanical Systems (MEMS) technologies to mobile devices, today’s smart devices are enabled with 3-axis accelerometers, 3-axis gyroscopes and 3-axis digital compasses, which taken together, provide nine DoF. The addition of a pressure sensor takes this number to ten DoF. Mobile devices also use proximity sensors to detect the presence of nearby objects (without physical contact) and ambient light sensors to minimize screen illumination and maximize battery life.

The main components of such devices consist of a Sensor Unit (SU), an Analog-to-Digital Converter (ADC), a Programmable Gain Amplifier, and an ASIC. These devices use I²C or SPI protocols to communicate spatial orientation to the external applications processor.

Traditional test versus sensor test

Traditional ATE tests such as open/short, leakage, power consumption and serial communication verification must be supplemented with tests specific to the broad spectrum of sensor devices being manufactured.

To reduce the footprint of the device, chip designers are limited by the number of pins available on the package. This restriction prevents test access to individual functional units within the chip, making it impossible to individually verify the functionality of the ADC or PGA. Therefore, test engineers use a System Level Test (SLT) approach wherein the device is tested as a complete system. The sensor is presented with a known stimulus level and the device response is monitored as a lumped element. System Level Testing deviates from standard ATE tests and pose challenges for the test engineer to develop appropriate stimulus for the type of sensor being tested.

After assembly and prior to test, the devices are considered “uncalibrated” or “raw devices”. As the devices go through the test, the device response is calibrated (trimmed) to produce a linear output in response to a linear input stimulus. Calibration improves the precision and accuracy of a sensor. During calibration, the gain of the device is trimmed by applying a known positive and negative stimulus to the sensor. The PGA gain settings are trimmed to meet device sensitivity requirements as specified in the data sheet.

The stimulus used for testing e-compasses is either a permanent magnet or an electro-magnet. To test an accelerometer or gyroscope, a known acceleration or angular velocity should be applied to the Device Under Test (DUT). A rate table is a stimulus whose angular velocity or position of the rate table. The DUT is placed on the rate table and as the table rotates the device is calibrated such that its output is directly proportional to the angular velocity of the rate table.

The first test engineering challenge is to maintain electrical contact with the DUT as it is being rotated. This poses a limitation as to the number of devices that can be simultaneously tested. The second test challenge is that the test engineer needs to use a reference device to determine the angular velocity or position of the rate table. The cost of the reference device is directly proportional to its precision. These references devices, therefore, pose challenges in minimizing the cost of test. In the case of an electronic compass, a precise magnetic field must be generated and then varied across the operating range of the DUT. With no available commercial solution for a 3-axis e-compass, Amkor’s test engineers developed a 3-axis stimulus, which eliminated moving parts.
by using precision wound coils, and allowed its customer to calibrate their 3-axis sensors in a single insertion.

Along with miniaturization, companies are focusing on developing combination sensors. For example, combining a gyroscope, accelerometer, e-compass and pressure sensor will provide the handset manufacturer with greater functionality in a smaller footprint. However, testing such combination sensors will require greater innovation from test development teams. Amkor has created a MEMS test development team focused on the integration and development of combinational sensor stimulus. This will eliminate multiple test insertions, reducing cost by enabling single insertion calibration to customers.

**Test to the rescue**

When a 3-axis sensor is assembled on the final printed circuit board, it is assumed that the package outline represents the sensor die orientation within the package. However, on examining the package outline drawings, a tolerance of +/- 0.1mm on the package is not atypical. However, this can result in a 6 to 8 degree positional error between the package and the device. Additionally, during die attach, the X and Y axis of the sensor may be slightly rotated to the package edge, adding to the error factor as shown in Figure 2. These unavoidable mechanical tolerances can cause high fallout due to compounded positional inaccuracy. Powerful algorithms in test can compute the die to package, package to test socket, and test socket to stimulus errors and create correction values that meet or exceed data sheet accuracy specifications. In 3-axis "e-compass" applications, when the customer device had a 0.5 degree accuracy requirement, through these cross-axis calibrations, Amkor has demonstrated reducing the error from 5 degrees to 0.2 degrees, allowing for 0.3 degrees of error in the assembly equipment used during the final assembly of the smart phone.

**Conclusion**

Test is usually associated as the step that detects and rejects parts due to electrical or mechanical process variations that reduce yield. As demonstrated above, the test process can improve yield through the recovery of parts that had poorer sensitivity by adjusting the PGA registers. By using powerful algorithms, test can compensate for rotational errors caused by assembly equipment, and recover parts that would have normally failed to meet accuracy requirements.

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**Figure 2. Illustration of DUT positional error within the test socket. (Courtesy of Amkor Technology)**

\[
\begin{align*}
& a = 1.4066 \\
& a + b + b - 2.125 \\
& c + d = 1.9 \\
& \tan(\theta + \varphi) = \frac{b}{a + b} \\
& \tan(\varphi) = \frac{d}{c} \\
& (a + b)^2 + b^2 = c^2 + d^2 - e^2 \\
& \text{Six equations: Six unknowns} \\
& \implies \theta \approx 8.29^\circ
\end{align*}
\]

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**Gerard John, Director, Test Development Group, Amkor Technology**

Gerard currently leads a team that designs, develops, and delivers test solutions to high volume manufacturing facilities in Asia. His past experience includes positions at Conexant Systems, Flarion Technologies/Qualcomm, and Motorola. Gerard holds a degree in electronics and telecommunications from Osmania University and an MBA from Gaine School of Business in Michigan.

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WHAT’S INSIDE?

POSSUM™ die design as a low cost 3D packaging alternative

The trend toward 3D system integration in a small form factor has accelerated even more with the introduction of smartphones and tablets.

Integration has focused on (a) reduced form factor in the X, Y, and Z dimensions, (b) more functions combined within a single package, and (c) improved electrical and thermal performance (reduced electrical and parasitic resistance and lower energy consumption). 3D integration must address the device, package and system roadmaps at a cost that promotes a healthy adoption curve. This area of semiconductor packaging is generating a great deal of research and development with high expectations for acceptance once the technology can meet price penetration targets.

3D system integration at the package level can be a more cost effective approach, providing greater design flexibility than at the die level, where multi-functional integration does not necessarily scale equivalently in terms of cost/performance by node. Some of the popular packaging approaches driving 3D integration include Package on Package (PoP), 3D die stacks using wire bonding, and 3D die stacks using Through Silicon Vias (TSV) and flip chip assembly. TSV is one of the most active areas of research and development in semiconductor packaging with significant revenues projected over the next 5-10 years in anticipation of its commercialization. TSV implementation requires considerable commitment in terms of expensive capital investment in equipment and tooling — from wafer handling to stacked assembly and test. Fabrication steps, such as etching through the holes on the back of the wafer, also add significant cost to the final assembly.

To present customers with 3D integration advances at a price that allows them to compete in their target markets today, Amkor has leveraged our expertise with Chip-on-Chip (CoC) and face-to-face device integration to promote the POSSUM™ chip attach methodology. Amkor has spent three years developing and implementing various CoC face-to-face technologies. There is much interest from the microelectronics community because of the modular approach to die integration, the ability to preserve speed and bandwidth without introducing excessive latency or parasitics, and the lower costs involved to produce effective 3D solutions for today’s products.

Face-to-face chip-on-chip technology

There are many ways to stack die:

• Face-to-face IC assembly is the joining of two or more dies with their final metal circuitry facing each other. Joining is done through flip chip assembly as opposed to wire bonding.
• CoC assembly where both dies face up in a pyramid configuration (small on top of large) has the top die wire bonded to the bottom die or substrate. The bottom die would also be wire bonded to the substrate.
• CoC assembly where the bottom die faces the substrate and mounted through flip chip attach, has the top die mounted facing up and, again, is wire bonded to the substrate (unless the bottom die contains TSVs).

“...assembly technology changes the thinking surrounding functional integration tactics,” explains Jemmy Sutanto, Amkor Technology.

Figure 1. Conceptual illustration of a POSSUM™ assembly where the daughter die is mounted face-to-face with the larger mother die. The mother die is then flip chip mounted onto a substrate or board. (Courtesy of Amkor Technology)
Customer adoption of all three forms of CoC assembly has been well received. However, in order to get the closest connection between the active circuitry on each die without the expense of introducing TSV processing, the face-to-face configuration is employed. It is being sought in markets as diverse as automotive sensors, logic and memory, MEMS (timers, accelerometers, gyroscopes), optoelectronics and microcontrollers. This is because it uses the existing chip attach or thermocompression (TC) infrastructure and can be ramped to HVM without complex wafer handling processes, making the cost less expensive than TSV approaches. Although it is not a TSV replacement, it enables high performance integration today and will be an adjunct to full TSV integration tomorrow.

The POSSuM™ assembly approach

The POSSuM™ stacked die configuration describes two or more devices assembled face-to-face where a smaller die is nested within 1/0-free areas of the larger die. The larger of the two dies is referred to as the mother die and the smaller one is called the daughter die. As shown in Figure 1, the daughter die is flip chip mounted onto the face of the mother die so as not to interfere with the mother’s surrounding flip chip bump pattern. The POSSuM™ assembly can be mounted onto a substrate as a CSP or BGA. It can also be mounted within a lead frame package or directly onto the PCB as a WLCSP.

Flip chip face-to-face processes are relatively simple. The flip chip bumps are applied to both mother and daughter dies followed by Wafer Backgrinding (WBG) and dicing. In addition, the mother die can be singulated or can remain in wafer form depending upon the optimized process flow. The daughter die is thinned and joined to the mother die through copper pillar micro-bumps. The combined height of the copper pillar micro-bumps plus the daughter die thickness is designed to be less than the collapsed flip chip bump that surrounds the daughter die. This is to enable sufficient assembly clearance between the daughter die and the next assembly surface. The choice of interconnect technology, whether copper pillar, solder ball or new material interconnect is chosen to accommodate the structural and performance requirements of the stacked multi-die system.

The copper pillar micro-bumps are currently in HVM production at 40µm/80µm staggered pitch and LVM at 30µm/60µm staggered pitch. Two different chip attach assembly processes have been adapted for face-to-face copper pillar bonding:

1. **MR-CUF**: Mass Reflow with Capillary Underfill has been used for pitch >80µm although this is being extended to 50µm capability. Capillary underfills have filled solder joint gaps between 30µm-50µm on POSSuM™ attached mother and daughter dies.

2. **TC+NCP**: Thermocompression bonding with Non-Conductive Paste is currently used in HVM production for die with pitch <80µm. Mass reflow has the advantage of self alignment of the solder bumps during solder reflow while TC+NCP has been found to be a very high yielding and extremely reliable process for finer pitch devices. In addition, thermocompression bonding is a preferred assembly process for devices that may otherwise be compromised by the use of underfills, mold compounds or other material sets that would fill the entire chip-to-chip gap.

Bump technologies that have been developed for the POSSuM™ assembly methodology include conventional copper pillar micro-bumps and SnAg solder bumps. Other interconnect structures that are being pursued involve chip attach structures chosen to provide for a given combination of stand-off, reliability, electrical or thermal properties.

Amkor has tested POSSuM™ assemblies using both similar and dissimilar bump technologies. Examples of similar bumping technologies are plated copper pillar micro-bumps (plated Cu+SnAg cap), plated SnAg solder bumps or pre-formed SnAg solder balls. Packages using Cu+SnAg have passed -55 to 125°C for 2000 temperature cycles (JESD22-A104D, Level B) and packages incorporating dissimilar bump technologies (ex: Ni+SnAg joined to Cu+SnAg bumps) have passed aggressive customer temp cycle testing at -55 to 155°C for 2000 cycles. Examples of interconnect approaches involving dissimilar materials might involve bump structures comprised of non-collapsible core materials to achieve desired spacing and electrical characteristics.

As expected with any new assembly approach, as various stacked constructions are investigated, they are modeled and tested to meet reliability standards. Once feasibility is demonstrated and the structure is characterized and qualified, it is then released to operations to implement a high yielding and production worthy HVM process.

The double POSSuM™ approach for dense 3D packaging without TSVs

The chip-on-chip face-to-face POSSuM™ design is very attractive to 3D integration because it provides:

- A close coupling (shorter, faster) communication path between mother and daughter die,
- Less inductance, cross talk and parasitic resistance than wire bonding (providing for high frequency applications and wider bandwidth),
- Improved heat dissipation through an integrated heat spreader (IHS).

Figure 2 illustrates a Double-POSSuM™ package. The Double-POSSuM™ design is actually defined by two levels of nesting die. The daughter die (red) is flip chip attached to the mother die (blue) which is then attached to another silicon die (yellow) instead of a substrate or board. This largest die is then flip chip attached to the substrate or board. The levels of nesting are dependent upon the overall profile of each assembled die, including warpage factors and the inclusion of any added materials such as non-conductive pastes, underfills, mold compounds, etc.

In Figure 2, three daughter dies are copper pillar micro-bumped and assembled onto the mother die. The mother die shows three rows of perimeter pitch solder bumps that are taller than the assembled daughter die to provide sufficient clearance to the next die, substrate or board surface — in this case, the largest (yellow) die that is flip chip attached onto a substrate. This large die then becomes the (grand)mother die of the newly defined structure. Several aspects of this construction are patent pending.
The POSSUM™ assembly as a game changer for MEMS packaging

The Double-POSSUM™ design can be applied to MEMS devices to create 3D integrated systems without relying on the presence of TSVs. Instead, the innovative package design will provide the close die-to-die coupling necessary for the high frequency demands of the system. Current MEMS packaging still uses wire bonding where hybrid capped MEMS and ASICs are assembled side-by-side in a single package. To reduce footprint and preserve signal integrity, variations of the POSSUM™ packaging approach are being considered, including the Double-POSSUM™ design. When working with high frequency oscillators, accelerometers or gyroscopes, roadmaps for MEMS packaging look ahead 5-10 years. The current use of wire bonds to connect the MEMS device with an ASIC increases cross talk and parasitic resistance. Instead, a MEMS die (or array) can be thinned and flip chipped on top of an ASIC. Copper pillar technology also allows for more I/O connections which means that multiple devices can be can be assembled within a given level of the nested stack. In this example, one or more MEMS die can be assembled onto an ASIC together with memory die, microcontrollers, etc. to realize 3D system integration at the packaging level similar to Figure 2.

Summary

The creation of chip-on-chip solder joints are exceptionally high yielding processes that also pass high reliability JEDEC testing. They provide the foundation for innovative 3D packaging approaches such as the POSSUM™ face-to-face, low profile stack or more complex nested POSSUM™ assemblies. Face-to-face bonding, whether incorporated into die-to-die or die-to-wafer process flows, extends system design options. The POSSUM™ assembly technology changes the thinking surrounding functional integration tactics. Tradeoffs between SoC and SIP approaches from a total cost of ownership perspective have long term and profound roadmap implications. The POSSUM™ packaging approach offers an alternate form of high speed, high signal integrity, die-to-die communication that does not need to be supported through a silicon interposer or TSVs. The technology is expected to compliment and extend TSV packaging approaches in the future while providing for a less costly interconnection methodology for nearer term requirements.
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KEYNOTES

• Perspectives on 3D TSV Benefits in Microelectronics Applications
  Laurent Malier, CEO, CEA-LETI

• Advancing high performance heterogeneous integration through die stacking
  Suresh Ramalingam, Senior Director Packaging and Advanced Technology Development, Xilinx

• The Future of Packaging: Advanced System Integration
  Ron Huemoeller, Senior VP Advanced Product Development, AMKOR

• 3D Integration for Mobile Applications
  Georg Kimmich, Head of Silicon Packaging R&D, ST-Ericsson

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OSAT positioning in the emerging Mid-End: Fan Out, 3D ICS and 2.5D multi die interposers

The historical regularity of technological advancement, driving the expansion of functions on a chip at a lower cost per function and lower power per transistor has changed. The cost benefit traditionally seen through the effort of technology scaling is no longer being realized. Both 20nm and 14nm technology nodes are no longer seeing the same cost benefit as in previous node advancements. In a reversal of cost fortune, the industry is now experiencing a wafer price increase, which in turn is altering the approach to the scaling.

One of the critical issues in SoC is the signal delay caused by on-chip interconnect parasitics. Another issue is that SoC approaches often require different foundry technologies to be integrated on the same IC. One solution, Through Silicon Via (TSV) provides the advantages of high-density, high-bandwidth connections between side-by-side die. It has also served well to accelerate the migration of packaging technology from a single die package platform to a multi die package platform, using the packaged multi die module as the backbone integrator as opposed to a motherboard. In doing so, a higher level of system integration is enabled providing opportunity for performance, profile and system level cost benefits. Package platforms such as ‘Wafer Level Fan-Out’ and ‘Through Silicon Via’ have been the primary enablers facilitating this active migration from board level systems to package level systems.

First, Amkor adapted existing bump and assembly equipment to create its baseline 200mm WLFO platform. Amkor then supplemented these existing assets with readily available 200mm systems from external sources. This has resulted in a cost-effective and extendable WLFO bump and assembly platform for initial process and package development. This “invest smart” strategy has allowed Amkor to minimize capital expenditures while advancing the emerging wafer level fan-out packaging technology to support the demands of high performance mobile and networking devices. In addition, Amkor has been able to optimize its WLFO process technology and assembly yields on the smaller and the more robust 200mm format before moving to a more capital intensive and challenging 300mm or panel-based infrastructure.

The timing of Amkor’s entrance into wafer level fan-out packaging is also a crucial part of its overall business strategy. Engagements with key alpha customers in strategic market segments will allow Amkor to support a wide range of products.
as applications arise in the mobile and networking arena, including Amkor’s single die one-layer RDL package. This baseline structure is targeted to support mobile data modems, power management ICs, CODECs, RF switches, and power amplifiers for mobile devices. It provides improvement in form factor, interconnect density, and electrical performance.

In addition to establishing a strong technical and business platform for single die wafer level fan-out, Amkor is extending the single die wafer level fan-out platform to accommodate increasingly desired advanced 3D structures. Amkor’s key enabling technologies, such as Through-Mold Via™ (TMV™), Chip-on-Chip (CoC), and Fine Pitch Copper Pillar (FP CuP), extend the single die wafer level fan-out application space beyond simple 2D structures. For example, TMV™ provides the most space efficient interconnect for unique 3D products such as sensing devices, where miniaturization is critical for mobile applications (see Figure 1).

Amkor’s first WLFO sensing device is scheduled to go into production in 2013. TMV™ is one of the enabling technologies to create WLFO Package-on-Package (PoP) structures, resulting in significant z-height reduction, improved electrical performance and a higher level of package integration due to the intrinsic benefits brought to the industry by wafer level fan-out.

Finally, CoC, coupled with FP CuP, allows memory and logic devices to be attached face-to-face in a POSSUM™ mounted wafer level fan-out structure, providing the most optimum low-latency electrical interconnect for mobile computing and networking applications. Amkor’s first POSSUM™ mounted logic-memory networking device will be qualified for release to production in 2013. Amkor’s rapid development cycle, robust assembly platform, and quick time to market continue to provide a path to rapid return on its WLFO investment.

**3DIC TSV**

The 3D TSV product sector represents the long-term goal of many products and applications to maximize package level integration. The full stack of logic and memory, and the multitude of combinations thereof, provide the ideal path for high performance applications. 3D stacking today is primarily represented by mobile and memory application spaces for high end products. Fine pitch copper pillar product development provides the foundations for TSV assembly development. Management of interactions between silicon, process and materials allows for integration of logic and memory. Amkor’s leadership position in the space of fine pitch copper pillar has provided rapid development of the TSV assembly process. From the logistics perspective, Amkor is committed to the OSAT MEOL (Middle End Of Line) wafer finishing model, where wafers are supplied full thickness. Wafer bumping followed by the backside wafer processing is completed in the Amkor K4 state-of-the-art facility in Gwangju, South Korea.

Amkor has pioneered development of multi die stacking (2 die and 4 die) for the memory industry and has engaged with multiple customers on development of application processors with memory products (single die and cube formats). Currently, three variants are offered including a standard over molded package and two versions with copper heat spreaders. The sequence for heat spreader attach, before or after mold, represents the final two more prevalent options. Each package offers pros and cons depending on end product thermal requirements. Figure 2 represents typical package configurations in the 3D application processor space.

The assembly process leverages fine pitch copper pillar products that are in high volume production utilizing Thermo Compression bonding with Non Conductive Polymer with non conductive polymer (TC+NCP) in the die 1 to substrate interconnection and a similar bonding process for the die 2 (memory) to die 1 bond. It should be noted that the die to die bonding process, although similar, utilizes a modified bump construction as outlined by the JEDEC wide I/O memory specification. Advanced materials such as advanced NCPs and film based non-conductive films (NCF) are also utilized to achieve product requirements.

Amkor has completed the installation and qualification of a turnkey MEOL wafer processing cell in the K4 (Gwangju, Korea) factory and is now working towards product qualification with several major customers. Over the past year Amkor has processed 1000’s of TSV bearing wafers through their MEOL. Amkor’s ability to support customers with both assembly and engineering services, such as electromigration and board level testing, from both the Seoul Korea and the Chandler Arizona based labs provides added benefit to their customer base.

**2.5D multi die TSV**

The 2.5D multi die interposer solution provides a crucial intermediate step for next generation products to allow side-by-side integration of technology optimized devices ahead of a full 3D assembly. Interposers allow massive wide parallel busses between memory and logic devices, improving speed and significantly reducing power consumption. System designs can move from a “system on a chip” to a multichip module with heterogeneous die optimized for a particular technology and connected by means of an interposer. A large die can also be partitioned into smaller die for improved silicon foundry yield then connected with an interposer. An added benefit of using an interposer between the advanced silicon node logic and the substrate is a stress buffer for CTE mismatch.

The interposer size in most cases is greater than 22mm per side and, in some designs, at the foundry reticle window of 26mm x 32mm. The thickness for these larger interposers is typically 100um with 10um TSVs. The large size combined with the reduced die thickness may result in higher warpage significantly impacting the assembly process. As a result, material and process selections become a key consideration in creating a high yielding, multi die stacked product. The common
is 2-6, each with 1K–40K copper pillar connections, assembled to interposers with 5K–20K solder bump connections, and mounted on a substrate that is 35mm–55mm on a side. An example of a typical product is shown in Figure 3.

The technology integration for large 2.5D multi die package assembly is extensive. The technology challenges include 40um pitch assembly, 300mm thin wafers, large flip chip assembly, minimal die to die spacing, die stacking, system warpage, system thermal challenges, and overall reliability. Different process options and die attach sequences for interposer to substrate and chips to interposer are used to balance design needs. The assembly methods for attaching multiple die with tens of thousands of I/O at 40um fine pitch require careful consideration of the die size and interposer warpage. Product design requirements may also dictate that the optimum assembly approach is achieved by combining methods such as mass reflow and thermocompression bonding for die attach and underfill. Test considerations at intermediate assembly steps are also considered for feasibility in the overall process flow. The key requirement for successful assembly is flexibility in the process and materials to meet all of the various product needs.

An example of a specific requirement today includes a customer requirement of electrical test of the logic die following attachment to the package prior to the addition of expensive customized memory. The optimum flow in this case could require that the interposer is attached to the substrate first, the logic is then attached to the interposer and the subsystem is tested from the BGA side. Following test, the memory is then added to the interposer, followed by final packaging, complete with final test. Another example of a highly integrated 2.5D multi die structure includes a deconstructed SoC die to improve foundry yield issues at the most advanced silicon nodes, requiring intimate die to die spacing, and as a result, specialized underfill material and application processing.

To meet customer product requirements for 2.5D assembly, material understanding and process flexibility is a must. Managing the warpage on a large 100um thick interposer through the process stages will continue to be a leading consideration. Providing interconnect for tens of thousands of I/O at 40um pitch or less will also continue to be a key driver for a material and process selection. Balancing these requirements allows customers to have massive interconnect without the yield or technology limitations of system on a chip. Amkor is poised to support the future of both 2.5D and 3D TSV products with strong capability, experience and continued investments in through silicon via packaging capability.

Conclusion

The semiconductor industry continues to experience a greater desire to integrate technology at the packaging level to help mitigate the cost penalty at the most advanced silicon nodes. TSV has been the primary impetus, by departitioning portions of the SoC into lower node technologies where possible and reconstructing into a multi die packaged modular system. This has aided in reducing complexity, mask layer count, wafer start cost and improving the wafer yield of the newer process nodes. However, it has ultimately provided the coveted path towards miniaturization, increased functionality, and more storage capacity at the package level.
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**Status of copper wire bonding**

In the second half of this decade, copper (Cu) is forecasted to become the dominant wire bonding material for semiconductor packaging, accounting for 80% market share. Today, it is estimated that copper or Palladium Coated Copper (PCC) wire is employed in over 20% of all wire bonded devices and will surpass the 50% mark within the next two years. For this article, reference to copper wire includes bare copper, PCC and similar derivatives.

**Ramping the technology**

Well over a decade ago, a select number of IDMs and OSATs started investigating copper as a replacement for gold wire. Throughout the supply chain, both wire providers and wire bonder equipment manufacturers (e.g. Kulicke & Soffa/Heraeus, et al.) started aggressively developing processes and bonders in anticipation of future industry conversion. Kulicke & Soffa states that 90% of their machines shipped last quarter were copper capable. STMicroelectronics recently reported cumulative shipments of 10 billion semiconductor packages with copper wire, initially utilized in power packages and today found in products such as set-top boxes, wireless, tablets and consumer devices. Texas Instruments announced shipments of 7 billion units in its analog, embedded processing, and wireless products. High Volume Manufacturing (HVM) announcements such as these, reflecting a comfortable level of process maturity, have been well received throughout the industry. Likewise, the major OSATs are shipping a large variety of laminate and lead frame packages in high volume. Copper wire assembly is qualified and in high volume production on all package platforms at each one of Amkor’s seven factories located in Korea, Taiwan, China, Japan and the Philippines. Amkor’s product portfolio of qualified package platforms is currently the broadest in the industry (Figure 1).

**Today’s copper wire bonding programs**

High volume copper wire production has been established across many product platforms and the industry’s sights are now set on next generation capabilities. A large percentage of early industry production included products with shorter lifetimes and less demanding reliability requirements. Today, high reliability standards and package complexity are the new units of measure for copper wire bonded products. Where are the OSATs positioned in terms of their ability to handle stringent reliability standards, die-to-die bonding, stacked die bonding, ultra-thin wire diameters, or bonding to next generation silicon?

**Rigorous automotive qualification takes copper wire bonding to a new level**

Caution and stringent qualification practices have long been associated with automotive applications and acceptance of copper wire has been a slow and methodical process. AEC-Q100 is a critical stress test qualification for automotive integrated circuits. Amkor is currently qualified to the Automotive Electronics Council’s AEC-Q100 specification for Grade 1 laminate products and production commenced earlier this year. The more severe AEC-Q100 Grade 0 requirement is presently under qualification. The qualified Level 1 laminate

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**Figure 1. Copper wire qualification history. Development began in 2001 with high volume SOIC production commencing in 2006. Today, Amkor is addressing highly complex multi-die configurations (die-to-die, stacked), ultra-thin wire, and qualification on next generation materials and Si nodes. (Courtesy of Amkor Technology)**
CABGA (a.k.a. FBGA) package employs 1.0mil bare copper wire bonded on a gold flash over a palladium bond pad. Copper wire provides for better heat dissipation while maintaining slow intermetallic (IMC) formation, extending Mean Time To Failure (MTTF). Copper wire conversion is being seriously evaluated for devices such as engine controllers. However, while much of the current focus is targeted to non-safety applications, downstream demands for improved thermal performance and higher temperature capabilities continue to drive interest within this industry. Conversion to copper will take longer in high reliability/high temperature applications where more reliability and performance data needs to be generated.

**Die-to-die bonding drives lower cost SiP and stacked construction**

One of the more challenging copper wire processes is die-to-die bonding. Ball bonding is typically defined by the creation of a first bond on the die through the formation of a Free Air Ball (FAB), followed by the shaping of a wire loop, and then the creation of a second bond onto a lead or substrate. To generate the FAB of the first bond, a high voltage spark is used to melt the tip of the copper wire to form the ball (as with gold wire). However, since copper is highly reactive to oxygen, it also requires the addition of a localized forming gas atmosphere (nitrogen and hydrogen) to prevent oxidation during bond formation. To complicate matters even more, when joining the second bond to another IC instead of to a lead or substrate, another FAB must be created and placed on the second die with the wire loop then bonded on top of this ball bond. Referred to as a Stand-off Stitch Bond (SSB), this two-step second bond process further increases the complexity of using the stiffer copper or PCC materials. However, even though the process is more complex, SSBs have been optimized for die-to-die copper wire bonding and are enabling the construction of a variety of multi-die structures. Because SSBs can also form very low loop heights, they are used for stacked die wire bonding as well. Figure 2(a) shows a photo of a die-to-die pyramid stack using PCC wire and stand-off stitch bonding. Figure 2(b) illustrates fairly dense three-tier looping and Figure 2(c) shows both die-to-die and die to lead frame bonding in a single MicroLeadFrame® (QFN) package. Figure 2(d) shows an SOIC assembled with 2.0mil bare copper and down bond.

**Ultra-low profile wire bonding facilitates stacking options**

Film Over Wire (FOW) materials are gaining interest for same size die stacks and reverse die stacks (where the top die is larger than the bottom die) as shown in Figure 3(a) and 3(b). For the two illustrations, die-to-die spacing defines the constraints of the bonding parameters. In Figure 3(b), the overhang length and thickness of the die also impacts the bonding parameters. In both cases, the goal is to remove silicon spacers between the die. In the case of 3(b), bonding “bounce” (or rebound) must also be eliminated to avoid initiation of micro-cracks or insufficient stability to create a secure bond. Although FOW is a more expensive material, ultra-low profile copper bonds and extra long wire loops are supported through this technology. Because the film has a thickness of 60 µm, the loop height is targeted to <50µm. Amkor employs 0.7mil palladium coated copper to address these bonding loop height constraints. In a recent qualification, an overhang die with a length of 2.0mm and a die thickness of 5mil passed all JEDEC Level 3 reliability tests.

**The Pin Gate Mold (PGM) PBGA offers an ideal cost reduction opportunity**

As discussed in the PGM PGBA article within this issue, by moving the corner gate to the center of a PBGA, wire sweep is significantly reduced. This allows for much longer and thinner wire bonds to be used without concern of shorting. The process is so well controlled that wire lengths upward of 250mils with a 0.7mil wire diameter are supported. Figure 2(b) illustrates a SEM of a three-tier design utilized in a PGM PBGA taking full advantage...
of its unique construction. Extending wire bonding capability within the PBGA platform pushes out the forecast for conversion to flip chip for next generation process nodes.

Summary

The market acceptance of copper wire has rapidly increased as early adopters are now in HVM. Amkor supports copper wire implementation across a broad segment of customers, end applications and geographic regions. Bare copper or PCC wire are in HVM for all standard package platforms with wire diameters from 0.6-2.0mils qualified on process nodes down to 40nm. Processes for 28nm nodes are currently in qualification, with 22nm nodes targeted for 2013.

A database of qualified pad structures representing numerous wafer fabs (including TSMC, UMC, GLOBALFOUNDRIES, SMIC, Dongbu, and IDMs, etc.) is maintained and up-front characterization to establish bond parameters is provided as a best practice.

Amkor continues to build upon its broad based production, from single die packages to complex multi/stacked die structures. The rise of leadless lead frame packages such as the MLF® (aka QFN) and SON are extending wirebonding down the technology curve. Similarly, refinements of the PBGA and the increased use of multi-chip and system in package (SiP) approaches are also fueling the wire bonding curve. Next generation programs include low loop bonding, die-to-die and stacked die bonding in numerous configurations. Qualification programs through HVM production on products addressing more risk adverse markets such as automotive applications continue.

Copper wire bonding provides a number of advantages to semiconductor packaging once the assembly learning curve has passed and reliable, high yield processes have been established. (Courtesy of Amkor Technology)

Copper has a number of excellent intrinsic properties that provide benefits to semiconductor assembly and packaging. And although copper wire will eventually displace gold for the lion’s share of downstream wire bonded processes, it will not be a solution for all semiconductor devices. It took the rising price of gold, continuous technology advancements, and the continued use of lead frame based ICs to finally drive the semiconductor industry to optimize wire bonding for copper. Years of concerted development by wire manufacturers, equipment makers, semiconductor designers, foundries, and OSAIs have been invested to bring copper wire bonding to its current level of maturity.

Copper is a harder and stiffer material than aluminum or gold, and much more brittle. Therefore, when combining ultrasonic energy, heat and pressure, the more forceful thermosonic bonding process required for copper wire attach can induce damage to bond pads and fragile Inner-Layer Dielectrics (ILD). The higher force of thermosonic bonding can also cause the top aluminum layer of the pad to splash out beyond the end of the bond. The upside of this process is that once the copper bonds are created, they are much stronger and more mechanically stable than gold or aluminum, even in high stress environments.

To help mitigate damage to under-pad circuitry, post-fabout wafer processing can include the placement of additional metal layers on top of final metal bond pads. This approach absorbs mechanical stress during the copper bonding process. Over Pad Metallization (OPM) is typically administered through IDMs and OSAIs that maintain bumping lines. Several package types such as TSSOP and MLF are in high volume production with OPM and redistributed circuitry at Amkor.

Copper wire is thermally stable and it has a high current carrying capacity which is attractive for power devices. It can pull heat away from the die which leads to improved performance at elevated temperatures. Copper wire also has lower resistivity (higher conductivity) than gold. This can lead to higher product performance in digital, high current mixed-signal and power applications. In some applications, copper’s high current carrying capacity allows for the elimination of wires that would otherwise be required when gold is used.

In addition, the bond between copper and aluminum final metal pads is less likely to exhibit Kirkendall voiding, which is important for finer diameter wires.

2 Private communication with Bob Chylak, Kulicke and Soffa Industries, November 2012.

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Deborah S. Patterson, Senior Director,
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Deborah joined Amkor in 2011. She is responsible for strategic and tactical marketing, and marketing communications. Prior to joining Amkor, Deborah provided business development, marketing and product management services through her company, the Patterson Group, LLC. Deborah has held various director level positions at Advantest, Kulicke and Soffa, Flip Chip Technologies, and StratEdge Corporation. She holds 5 US Patents in microwave packaging and filters for satellite communications. Deborah holds an electrical engineering degree from the University of California, San Diego and a biology degree from Furman University.

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SungMoo is leading Amkor Cu wire qualification and technology improvement. He has more than 20 years experience in various packaging areas at Amkor. Prior to moving to the K4 plant, SungMoo was responsible for engineering in Amkor Philippines SIP and MENS packaging. He was also responsible for directing the wire bond process improvement council of ATK1 plant in Korea.

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Re-engineering the PBGA: changing the manufacturing process revamps old product to lower costs, extend to next generation nodes

Amkor took a new look at the old familiar Plastic Ball Grid Array (PBGA) to find ways to bring down costs, and found options as well to drive down wire diameter to extend wire bonding to the 28nm node and beyond.

Key to the new approach is moving the transfer mold gate from the corner to the center of the mold cap (Figure 1). That means the mold compound flows out parallel to the bonding wires, combing them in the desired direction instead of pushing them aside as the flow from the old corner gate tended to do. Since wire sweep is essentially eliminated, thinner diameter wire can be used, and wire lengths can be longer.

The longer wire bond length allows lower routing density on the substrate, or 60µm/60µm lines and spaces instead of 40µm/40µm, for lower costs. Amkor estimates that process improvements and the lower cost, lower density substrates can mean a 4%-6% savings without any changes to design or wire.

More savings, however, come from enabling the use of thinner wire. The center pin-gate approach allows use of gold wire as thin as 0.6mil in production today, with 0.5mil planned for next year. At 0.6mil, gold packaging cost can approach the same costs as packaging copper. Use of thinner gold wire, or switching to copper wire, can lower costs by an additional 10%-30%.

Optimizing the wire bond layout for the new platform, with higher densities and without the need to allow for wire sweep, has then allowed further reduction in wire length of up to 25%-50% on customer devices by using the latest substrate design rules.

The 0.7mil gold wire can have a maximum length of 250mils with the new pin-gate format, compared to the 1.2mil thickness necessary to get to that 250mil length using the standard corner-gate PBGA. Since the gold wire and the substrate account for some 75% of the cost of the conventional PBGA, these innovations have significant impact on the cost structure.

But equally significant may be how this apparently simple molding gate change also extends the mature wire bonding package to next generation higher density devices, as the higher densities of thinner wires can handle advanced silicon nodes with their smaller pad openings. That of course brings the potential to extend lower cost wire bonding further into what was once purely flip chip territory.

Amkor has produced more than 25 million pin-gate PBGA packages since beginning high volume production in 2009. It plans to convert all 19mm-31mm body size corner gate production to the new pin-gate version by the end of 1Q13 at its K4 plant.

Figure 1. (a, c) Conventional PBGA with corner gate, (b, d) PGM PBGA with center gate. The two packages on the right show the heat sink attached. (Courtesy of Amkor Technology)
Larger mold cap, switch to sawing improve yields

The center-gate approach also allows a larger mold cap and a smoother perimeter, which both contribute to better yields than the traditional package.

The larger cap’s coverage of more of the surface better protects the active traces and vias to minimize the risk of common problems of trace and solder mask cracking. The smaller exposed flange on the perimeter of the package is also more resistant to mechanical damage and bending.

The redesign of the traditional PBGA process also replaced traditional punch singulation with package sawing for smoother edges. The smoother edges are less likely to catch on test sockets or shipping trays, resulting in higher yields. Both standard PBGA and thermally enhanced TEPBGA-2 are now supported in the same mold systems, using the same mold tooling, further reducing cost of ownership.

The larger bond shell also enables larger die sizes, or more room for multichip layouts, and the overall marking area is larger.

Though the mold gate is located in the top center of the mold cap, a drop-in heat spreader can still be used, with the simple addition of a clearance hole in its center.

The larger mold cap has little impact on test equipment, board level reliability or warpage. Vacuum pick up tools that use the substrate edges for gross alignment need no changes, though those that use the side walls will need a minor modification.

Reliability of the pin-gate PBGA has been shown to be the same as corner gate packages by simulation, qualification and field data. Simulation of mean time to fatigue (50%) shows little difference between devices in the new, pin gate package with the larger mold cap and the traditional corner gate technology, for either the 12mm or 6mm die size.

Simulation also indicated little difference in warpage between pin gate and corner gate devices at 25°C. At reflow temperature (260°C) differences were also small, although the center-gate PBGA has slightly higher warpage than the corner gate version, while the thermally enhanced version had slightly lower warpage than the corner gate.

“For those automotive, military and industrial applications not yet ready to fully convert to copper wire bonding, Amkor’s pin-gate PBGA process is an opportunity to achieve copper-wire-like costs by using very thin gold wire,” explains Jeff Miks, Amkor Technology.
In summary, PBGA packages are a mature technology used in a wide range of applications ranging across markets such as computing, network infrastructure, gaming, set top boxes and digital TV. The new pin-gate approach improves this established product with improved performance, higher yields and lower cost, while extending the usefulness of wirebonding to smaller silicon nodes. For those automotive, military and industrial applications not yet ready to fully convert to copper wire bonding, Amkor’s pin-gate PGA process is an opportunity to achieve copper-wire-like costs by using very thin gold wire.

Jeff Miks, Senior Director, PBGA, DLP and Image Sensors, Amkor Technology

Jeff joined Amkor in 1999, and has served as the Business Unit Director for Game, Memory and I/O Card products as well as the Senior Manager of Lead Frame Products. Jeff has authored numerous technical publications in leading industry magazines, and holds eight patents with an additional 15 patents pending. Jeff holds a mechanical engineering degree from Colorado State University.
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Flip Chip Molded BGA (FCMBGA): enabling networks to mobile devices

The flip chip molded BGA (FCMBGA) is a semiconductor package that can produce a large, very thin and extremely flat platform that also delivers excellent electrical and thermal performance.

The FCMBGA’s unique benefits are sought after for applications as diverse as networking and storage to broadband communications and mobile devices.

What is it about this unique packaging approach that addresses such a wide-ranging spectrum of end-use applications?

The engineering and materials science that defines the FCMBGA provides for several important benefits. The FCMBGA is a package that can:

- enable coplanarity of very large and thin die,
- provide extremely efficient heat dissipation,
- increase electrical performance,
- increase structural reliability (especially for advanced silicon nodes that employ low-K dielectrics),
- provide the flexibility of reducing package footprint or increasing die size in the same footprint, and
- in certain applications, significantly reduce cost.

These benefits are a direct result of the processing technology itself. The FCMBGA is defined by an exposed die format as shown in Figure 1. The package uses a molding compound to assemble large die or multiple components onto BGA substrates without the structural need for a lid or stiffening ring.

A definitive feature of the FCMBGA is its ability to support larger die (≤20mm) on BGA substrates that measure from 15mm to 42.5mm while sustaining excellent coplanarity – even for very thin components, bare die or for thin core substrates.

Innovation through unconventional material choices

As many semiconductor engineers have learned, thin die will warp. As die get larger, warpage is exacerbated, and downstream processing can worsen the effect. Traditional capillary underfilled packages have reached reliability limits for larger and thinner die manufactured at ultra low-K nodes. The FCMBGA molding compound seen surrounding the die in Figure 1, but not encroaching upon it, replaces the capillary underfill used beneath the die. The molding compound locks the structure in place much like traditional underfill, extending solder joint reliability over a larger area. However, unlike underfilled materials, reliability is extended because the mold compound has a unique adhesive property. The mold compound employs a very fine filler particle size to ensure complete coverage in the small flip chip gap. Because of this fine filler particle size, it has higher filler content — roughly 80% filler material compared to 55-65% of traditional capillary underfill materials. The high filler content reduces moisture absorption and increases bonding between critical interfaces such as the substrate, bump, die and their varying surface treatments. The proprietary molding compound, therefore, provides increased rigidity, flatness and reliability to the structure, extending die size range for bare die packages that would otherwise require a stiffener and/or lid to meet JEDEC coplanarity requirements.

Case study: thermal enhancement and electrical improvement for networking and wired communications

The FCMBGA has been adopted for high-performance and low-cost applications with Field Programmable Gate Arrays (FPGA) being the first devices to go into production.

The packages are designed to allow for die protrusion over the mold cap, creating the thinnest bond line and best thermal impedance between the flip chip die and an attached heat sink. This retains the excellent thermal performance of bare die FCGBA configurations while providing a support surface around the die for the direct heat sink attach.

“"The FCMBGA’s unique benefits are sought after for applications as diverse as networking and storage to broadband communications and mobile devices,” says Deborah S. Patterson, Amkor Technology.
A lid or heat spreader attached to the exposed back of the die is optional, depending upon the thermal requirements of the device, ultimate ratio of thickness to footprint, and silicon construction. For small to medium die sizes of 8-14mm, the FCMBGA provides excellent coplanarity without the need for a stiffener/lid or formed lid. Elimination of the lid in favor of a direct heat sink attach can greatly reduce package cost (lid, TIM, assembly, etc.) while concurrently producing a thinner package.

For larger die sizes where trade-offs between heat sink and lid attach configurations are being considered, the FCMBGA offers the flexibility of attaching a lid to the structure. Figure 2 illustrates the cross-section of both the un-lidded and lidded options.

Aside from thermal considerations, there are several noteworthy electrical enhancements introduced through the molded underfill process flow and FCMBGA structure. Most significantly is the elimination of keep-out exclusion zones due to capillary underfill bleed. This allows decoupling capacitors to be mounted as close as possible to the die, always a welcome option for improved system performance and improved substrate real estate usage (which may translate into improved board real estate savings). Similarly, multichip SIP approaches requiring high levels of integration and the close coupling of die would be well supported for the class of products that do not require a high-end silicon interposer solution. The use of thinner substrates to support increased signal densities and less signal delay, along with the close coupling of die and passive components have resulted in (a) improved signal integrity for noise sensitive high-speed signals and (b) reduced signal lengths and power distribution for challenging signal and improved power integrity requirements.

The simultaneous assembly of peripheral passive components with active die, in addition to eliminating underfill dispense, also results in a lower cost assembly.

The FCMBGA supports ASICs, FPGAs, processors and GPUs in applications such as remote radio units, 10G/40G controllers and line cards or LANs. Telecommunications and networking present numerous opportunities for the FCMBGA. Ethernet routers and switches, servers and storage systems, and even GPUs for computing and gaming have need of the performance, power and integration provided by this packaging approach.

Case study: multi-use platform for mobile applications

The limitations or, indeed, the additional leverage that packaging contributes to system architecture choices, will directly influence our customers’ functional integration roadmaps. Semiconductor suppliers are examining System-On-Chip (SoC) tradeoffs — which functions should be integrated at which silicon nodes – against foundry roadmaps. This will be compared against System-in-Package (SiP) tradeoffs to calculate overall cost of ownership and interception points across multiple markets.

For example, GPS is presently being integrated with Wi-Fi, Bluetooth, and Frequency Modulation (FM) in some of today’s combo chips. These functions will next be combined with the application processor in premium smartphones and/or media tablets. Eventual incorporation of Near Field Communications (NFC) controllers are expected to follow. In parallel, RF and Front-End Modules (FEM) are candidates for integration with baseband processors, and eventually all of these functions may converge to find themselves in a single chip.¹

Add to this the considerations of inventory control, economies of scale and device interchangeability between platforms such as smartphones and media tablets, and the motivation to overlay packaging options against silicon roadmaps is understandable.

A popular example of leveraging economies of scale is Apple’s processor. In its current iteration, Apple employs the A5 in multiple product types, thereby increasing their purchasing leverage.

Figure 2. Cross-section of the FCMBGA showing (a) un-lidded and (b) lidded options. (Courtesy of Amkor Technology)
and reducing cost, streamlining their BOM (and commensurate internal costs), and building in systemic efficiency across their inventory and supply channels. Similarly, leveraging the FC*BGA across multiple devices or using it to enable interchangeability among end-use applications underlies the economies of scale in manufacturing and inventory control that contribute directly to the bottom line.

The motivation to leverage downstream SoC options is clear. However, enabling this path requires an assembly methodology that can support the fragile dielectrics of ultra low-k nodes combined with increasing footprint size and decreasing package thickness for use in multiple mobile applications. The FC*BGA is a serious packaging approach to be considered when analyzing cost of ownership scenarios for the mobile electronics markets.

**Attributes that impress**

Numerous advantages can be realized by transitioning to the FC*BGA. These include improved electrical performance through the use of thin cores/coreless substrates, closer placement of decoupling capacitors, and shorter interconnections combining improve signal integrity and signal densities. Structural benefits include impressive warpage control, large and thin platforms, efficient use of substrate real estate, and compatibility with low-k materials. Excellent reliability has been demonstrated.

Efficiencies of cost are attained through the simplified process flow, concurrent molding of multiple devices, optimized body size and ability to use un-lidded packages for direct heat dissipation or simply for cost savings.

The FC*BGA is commercialized using single piece processing on 4-10 layer build-up and coreless substrate materials. Die to substrate bumping includes eutectic, lead-free, and copper pillar micro-bumps. The FC*BGA is JEDEC MS-034 compliant at 0.8mm and 1.0mm BGA pitches for both eutectic and lead-free solder balls.


Deborah S. Patterson, Senior Director, Product and Technology Marketing, Amkor Technology Deborah joined Amkor in 2011. She is responsible for strategic and tactical marketing, and marketing communications. Prior to joining Amkor, Deborah provided business development, marketing and product management services through her company, the Patterson Group, LLC. Deborah has held various director level positions at Advantest, Kulicke and Soffa, Flip Chip Technologies, and StratEdge Corporation. She holds 5 US Patents in microwave packaging and filters for satellite communications. Deborah holds an electrical engineering degree from the University of California, San Diego and a biology degree from Furman University.

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Chip-Scale Packaging: processing, solutions and outlook

Over the past several decades in the microelectronics industry, one trend has been undeniable: miniaturization. Devices have gotten smaller, thinner, and lighter, without any accompanying degradation in quality, performance, or reliability. One reason for this success has been the broad acceptance and consistent advancement of Chip-Scale Packaging (CSP) solutions.

Chip-scale packaging has notoriously been an ambiguous term. Originally, CSPs were defined to be no greater than 20% larger than the die size. More recently, the definition has evolved to include packages with a form factor up to 2x the die size. Packages of this type are especially useful for application processors and other mid-power, high signal density devices. Given their relatively small form factor, CSPs are found in a multitude of consumer, embedded, and automotive products; everything from smartphones and tablets to industrial equipment and in-dash infotainment consoles.

There are a myriad of possible CSP designs, in both 2D and 3D constructions, all of which can be tailored to specific customer needs. Amkor offers unique flexibility in the design and assembly of CSPs to meet diverse technical and cost-based requirements. In the 2D space, bare-die and molded single-die wire-bond or flip-chip options are available, as are side-by-side multi-die constructions. These layouts allow several semiconductor devices to be integrated into a single package to meet reduced system-level spacing and electrical requirements. Stacked die constructions combining both wire-bond and flip chip technologies (a.k.a. FlipStack™) are also fully qualified, allowing devices with different final metal bump pad layouts to be packaged in a single unit. Baseband, logic, application processors, high-density flash and DRAM are some of the devices that benefit by incorporating these technologies.

The recent explosion of smartphones and tablets into the consumer market has led to rapid increases in I/O density for application processors, which in turn has increased demand for packaging solutions which can reliably accommodate stringent silicon design requirements. For this reason, the leading edge devices that power these products often incorporate flip chip technology for its improved electrical performance, reduced die footprint and profile, increased reliability and I/O flexibility. In particular, copper pillar flip chip is used in fine bump pitch devices (typically ≤150µm) since its stand-off height relative to its solder joint diameter prevents bump-to-bump shorting, as shown in Figure 1.

Copper pillar technology has many benefits, including excellent electromigration performance for high current-carrying applications, but it has also become a leading player in the industry’s miniaturization efforts. Bump pitches can be reduced to as low as 50µm in-line and 40/80µm staggered, with 25µm in-line pitch demonstrated but not in production. With such small bump pitches, substrate layer count can be reduced, lowering overall package heights and material costs. In addition, because Amkor’s copper pillar bump process allows for wafers to be probed before bump, known good die are identified before chip attach, thus decreasing overall test and assembly costs.

The advantages of copper pillar assembly extend far into the life of the end products themselves as well. Long known for their reliability, some copper
Pillar packages have gone as far as 6000x temperature cycles of IPC standard TC1 without fail, which is between 3-6x longer than most devices required for qualification, depending on final application (consumer vs. automotive application, for example).

A major advantage of copper pillar bumping exists for customers who are transitioning from wire-bond packaging to flip-chip packaging. Copper pillar assembly allows the chip design to maintain peripheral-based signal routing, without time-consuming redesign, thus accelerating time-to-market and reducing design costs. Copper pillar bumping is now being incorporated into package development for next-generation silicon nodes thanks to its strong track record, including hundreds of millions of units shipped to date by Amkor.

Three assembly processes provide a portfolio of tailored solutions

While copper pillar architecture has established itself as a robust, reliable fine-pitch packaging option, there are three predominant assembly processes which have been shown to cheaply and effectively produce high volumes of product: Thermo-Compression with Non-Conductive Paste (TC+NCP), Mass-Reflow with Capillary Underfill (MR-CuF), and Mass-Reflow with Mold Underfill (MR-MUF).

The TC+NCP process involves applying a non-conductive adhesive paste between the die and substrate, and then joining the bumped die to the substrate's flip-chip pads through high temperature and high pressure bonding. Much research has been devoted to this process in recent years, with particular focus on NCP material selection and bonding parameters. Aside from the benefit of finer bump pitch, TC+NCP can also accommodate very thin dies, 60µm and below, by way of wafer back-grinding.

While TC+NCP is best suited for the finest pitch devices, MR-CuF and MR-MUF are low-cost, reliable processes for die bonding when ultra-fine bump pitches are not required. This is often the case when the silicon device is designed with a full array of die bumps, instead of a predominantly peripheral design, but there is a large overlap wherein both mass reflow and TC+NCP are technically feasible. Cost is often the driving force in the end. As a general rule, in cases where bump pitch is above about 80µm, mass reflow is often the more suitable solution.

Capillary underfill relies on the application of an inert underfill material to provide stability and electrical isolation of I/Os. The underfill material is applied along a die edge and is transported via capillary action into the gaps between bumps under the die shadow. In many devices, a molding material is applied over the die to encase the whole package for further mechanical stability as well as to meet coplanarity and warpage requirements. In MR-MUF, the molding material is used to underfill the die, which simplifies processing and promotes better mechanical joints at the die-package interface. Processing benefits include fewer steps, fewer materials, and the ability to underfill a batch of substrates at once, versus the one-at-a-time processing that is typically required in TC+NCP and MR-CuF. This leads to cost reductions and higher factory through-put. Further, MR-MUF does not have an underfill fillet, which saves package space by reducing component keep-out zones needed for assembly.

Amkor has extensive experience in both thermo-compression and mass reflow processing technologies, and process selection depends on the packaging requirements. Amkor has demonstrated TC+NCP applications for bump pitches as low as 40/80µm staggered in High Volume Manufacturing (HVM) and 30/60µm staggered in development. Package sizes up to 16x16mm and die sizes up to 8mm on a side are in HVM, while even larger package sizes and die sizes are under qualification. Silicon nodes down to 28nm are also in HVM. Due to the low stress induced during bonding (compared with mass reflow), TC+NCP is especially applicable to next-generation silicon nodes that employ brittle low-k dielectrics coupled with ever larger and thinner dies.

TC+NCP, MR-CuF and MR-MUF have all passed rigorous reliability standards and have become standard architectures for fine pitch flip-chip products. Mold underfill is currently limited to bump pitches at or greater than 120µm, while capillary underfill can be used at bump pitches down to 80µm and lower, as well as in larger package sizes. Specific product applications dictate process choice on a case-by-case basis based on bump pitch and package size. There is significant overlap in the suitability of each process for a given solution, and in such cases, cost is the determining factor. These three assembly processes form a portfolio of tailored solutions that cover an increasingly wide array of customer requirements, and allow Amkor to avoid limitations due to bump pitch, die size or package size.

Through-Mold Via (TMV®) package-on-package as industry standard

For high-density Package-on-Package (PoP) applications, fine-pitch Ball Grid Arrays (BGA) at the interface of the top and bottom package are necessary, and to meet this demand, Amkor’s Through-Mold Via (TMV®) solution was developed. TMV® technology provides a method to solder two packages together through the bottom package's mold cap. A sample TMV® PoP design might couple a high-density application processor on the bottom with a stacked DDR or DRAM die in...
a single memory package on top. Because TMV® PoP requires only a mold cap be designed in the bottom package, it can be applied to nearly all bottom package designs, including stacked-die, FlipStack™, flip-chip, wire-bond, and through-silicon via packages.

The technical benefits of TMV® PoP improve Board-Level Reliability (BLR) and extend the Surface Mount Technology (SMT) process window. Because each interface ball between top and bottom package is mechanically isolated and supported around its circumference by the mold cap, as shown in Figure 2, the total package-to-package interface is stiffened against reflow-induced warpage. Meeting the demand for current and future memory package ball pitch, TMV® PoP interface pitch supports 0.4mm in HVM, and as low as 0.3mm in development. Solder ball size and mold cap height can be tailored to the specific package design requirements.

Now in HVM for over a year, TMV® PoP has become a de facto standard for high density PoP packages due to its attractive mechanical attributes and long-term reliability record. Additionally, like all PoP packages, TMV® gives end customers the flexibility to partner with several suppliers at once for top package supply. This allows for low-cost, high-availability top-packages to be coupled with the demonstrated technical capability of TMV® PoP to form a single low-cost, next-generation packaging solution for consumer or industrial applications.

Chip-scale packaging has become a bit of a buzzword in the microelectronics industry, due to a track record of providing highly capable solutions for many different silicon device requirements. Whether the die is large or small, whether bump pitch is wide or very fine, whether the package height must meet a new minimum threshold, it is clear that recent advances in processing technology have allowed new and more complex devices to be assembled in low-cost processes with high reliability. The diversity of end applications which benefit from chip-scale packaging not only ensures that today’s products are supplied with quality, dependable solutions, but that this trend will continue into the foreseeable future.
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